URN etd-0407109-183725-2055
Author Hao-Kai Liao
Author's Email Address No Public.
Statistics This thesis had been viewed 41 times. Download 22 times.
Department
Year 2001
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title Programmable Decimators and Interpolators for Sigma-Delta A/D and D/A Converters
Date of Defense 0000-00-00
Page Count 0

Keyword
Decimator
Interpolator
FIR Filter
Programmable

Abstract
A design technique of the programmable decimators and interpolators for sigma-delta analog-to-digital converters (SDADCs) and sigma-delta digital-to- analog converters (SDDACs) is presented in this thesis. The programmable decimators and interpolators consist of the programmable controller, the decimator and the interpolator. The decimator and the interpolator can share the hardware structures with four digital filters. A cascaded structure with four digital filters is used to construct the decimator and the interpolator, respectively. The decimator and the interpolator consist of a comb filter, two FIR filters, and a compensation filter. The decimator function is that the noise outside the signal band is attenuated and the input sampling data rate can be decreased, and the interpolator function is that the image outside the signal band is attenuated and input sampling data rate can be increased. A reduced-multiplier structure of FIR filter is presented and adopted to realize two FIR filters and a compensation filter. In addition, the programmable controller comprises the programmable decimation and interpolation rate controller and the programmable specification controller. The programmable decimation and interpolation rate controller is used to control the decimator and the interpolator for SDADCs and SDDACs with the various oversampling rates. The programmable specification controller is adopted to control the decimator and the interpolator for SDADCs and SDDACs with the various specifications. The simulation results reveal that the programmable decimators and interpolators can be applied to SDADCs and SDDACs with 32/64/128/256 oversampling rates, which can achieve 18-bit resolution.

In addition, in this thesis, a design technique of the decimation filter for SDADCs has been successfully fabricated. A fixed- coefficient multiplier structure is also developed and applied to the multipliers of the FIR filters. In the design, the TSMC 0.35μm, 1P4M digital CMOS process and Avant! 0.35μm cell library are used to fabrication. The simulation and measurement results reveal that the decimation filter can be applied to SDADCs with resolution over 9-bit.
Advisory Committee Shuenn-Yuh Lee - advisor

Files etd-0407109-183725-2055-001.pdf

indicate access worldwide
Date of Submission 2002-08-22